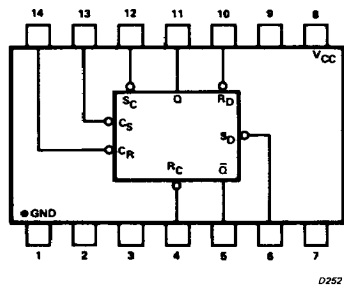


PIN CONFIGURATION



SP629A

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)
Standard Conditions: $V_{CC} = 5.0V$, $T_A =$ Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage "1" Level	$I_{out} = -200\mu A$, Driven Input	3.8			V
"0" Level	$I_{out} = 20mA$, Driven Input			0.6	V
	$I_{out} = 12.5mA$ Driven Input			0.4	
Input Current input high S_D , R_D , clock	$V_{in} = 5.0V$			25	μA
S_C , R_C	$V_{in} = 5.0V$			25	μA
input low S_D , R_D , S_C , R_C	$V_{in} = 0.6V$			-2.5	mA
Clock Effective Capacitor			75		pF
Power Supply Current	$V_{in} = 5.0V$, $T_A = 25^\circ C$			10	mA
Turn on Delay clocked	See Test Figure 1, $T_A = 25^\circ C$			100	ns
direct	See Test Figure 2, $T_A = 25^\circ C$			100	ns
Turn off Delay clocked	See Test Figure 1, $T_A = 25^\circ C$			100	ns
direct	See Test Figure 2, $T_A = 25^\circ C$			100	ns
Fan-out -To sink loads (2.5mA/load)				8	
-To source loads (180 μA /load)				1	

Typical Values are for $T_A = 25^\circ C$. See Page 3 for Notes.

8V V_{CC}

R_D 10

3.8K 4.2K 1.5K

1.5K 4.2K 3.8K

S_D 6

11

13.7K 13.7K

9.4K 9.4K

1

100 10K 10K 100

S_C 12

13 14 15

C_S C_R

4

R_C

Component Values are Typical

629A

D252

629A					
S_C	R_C	Q	S_D	R_D	Q
0	0	?	0	0	*
0	1	1	0	1	1
1	0	0	1	0	0
1	1	No Change	1	1	No Change

CLOCK SET/RESET

DIRECT SET/RESET

*Both Q and \bar{Q} remain in "1" state until S_D or R_D rises.

[illegible]

Figure 2 shows the timing diagram and circuit schematic for the 74ALS00. The schematic illustrates the clock input (C) connected to the S and R inputs of the NAND SR flip-flop. The clock input is driven by a pulse generator with a rise/fall time of 15 ns. The clock input is also connected to the inputs of two 387 inverters, which are configured as a NAND gate (380) and a NOR gate (380). The output of the NAND gate is connected to the Q output of the flip-flop, and the output of the NOR gate is connected to the Q-bar output of the flip-flop. The flip-flop is also connected to two 387 inverters, which are configured as a NAND gate (380) and a NOR gate (380). The output of the NAND gate is connected to the Q output of the flip-flop, and the output of the NOR gate is connected to the Q-bar output of the flip-flop. The timing diagram shows the clock input (C) and the Q and Q-bar outputs. The clock input is a square wave with a high level of 4.0V and a low level of 1.5V. The Q and Q-bar outputs are square waves with a high level of 1.5V and a low level of 1.5V. The timing diagram also shows the setup and hold times (t_{on} and t_{off}) for the Q and Q-bar outputs.